CLAIMS

What is claimed is:

1. A method for forming at least one non-volatile memory cell, comprising:
forming a component stack of the at least one non-volatile memory cell on a surface of a substrate, wherein the component stack comprises an electron trapping layer;
forming a dielectric layer over the component stack;
removing a portion of the dielectric layer such that a remainder of the dielectric layer exists substantially along sidewalls of the component stack;
forming an oxide layer over a bit line existing in the substrate adjacent to the component stack; and
forming a first electrically conductive layer over the component stack and the oxide layer.

2. The method as recited in claim 1, wherein the forming of an oxide layer over a bit line comprises growing an oxide layer over a bit line existing in the substrate adjacent to the component stack.

3. The method as recited in claim 1, wherein the remainder of the dielectric layer substantially prevents the oxide layer from extending under the component stack.

4. The method as recited in claim 1, wherein the electron trapping layer comprises silicon nitride.

5. The method as recited in claim 1, wherein the component stack further comprises a first dielectric layer and a second dielectric layer, and wherein the electron trapping layer is interposed between the first and second dielectric layers.

6. The method as recited in claim 5, wherein the component stack further comprises a second electrically conductive layer, and wherein the electron trapping layer is positioned between the second electrically conductive layer and the surface of the substrate.

7. The method as recited in claim 1, wherein the forming of a component stack comprises:

forming a first oxide layer, a nitride layer, a second oxide layer, and a second electrically conductive layer on a surface of a substrate in that order;

forming a patterned photoresist layer on the second electrically conductive layer; and

using the patterned photoresist layer as a mask to pattern the second electrically conductive layer, the second oxide layer, the nitride layer, and the first oxide layer.

8. A method for forming at least one non-volatile memory cell, comprising:

forming a first oxide layer, a nitride layer, a second oxide layer, and a first electrically conductive layer on a surface of a substrate in that order;

forming a patterned photoresist layer on the first electrically conductive layer;

using the patterned photoresist layer as an etching mask to form a component stack of the at least one non-volatile memory cell on the surface of the substrate;

using the patterned photoresist layer as a doping mask to form a bit line in the substrate adjacent to the component stack;

removing the patterned photoresist layer;

forming a dielectric layer over the component stack;

removing a portion of the dielectric layer such that a remainder of the dielectric layer exists substantially along sidewalls of the component stack;

forming an oxide layer over the bit line; and

forming an electrically conductive layer over the component stack and the oxide layer.

9. The method as recited in claim 8, wherein the forming of an oxide layer over the bit line comprises growing an oxide layer over the bit line.

10. The method as recited in claim 8, wherein the remainder of the dielectric layer substantially prevents the oxide layer from extending under the component stack.

11. The method as recited in claim 8, wherein the nitride layer comprises silicon nitride and forms an electron trapping layer.

12. The method as recited in claim 8, wherein the using of the patterned photoresist layer as an etching mask and the using of the patterned photoresist layer as a doping mask comprise:

using the patterned photoresist layer as an etching mask to pattern the first electrically conductive layer, the second oxide layer, and the nitride layer;

using the patterned photoresist layer as a doping mask to selectively introduce dopant atoms into the surface of substrate; and

using the patterned photoresist layer as an etching mask to pattern the first oxide layer.

13. A non-volatile memory cell, comprising:

a component stack arranged on a surface of a substrate, wherein the component stack comprises an electron trapping layer;

a plurality of dielectric spacers positioned along and in contact with sidewalls of the component stack;

an oxide layer positioned over and in contact with a bit line existing in the substrate adjacent to the component stack; and

a first electrically conductive layer positioned over and in contact with the component stack and the oxide layer.

14. The non-volatile memory cell as recited in claim 13, wherein the oxide layer is a grown oxide layer.

15. The non-volatile memory cell as recited in claim 13, wherein the dielectric spacers substantially prevent the oxide layer from extending under the component stack during formation of the oxide layer.

16. The non-volatile memory cell as recited in claim 13, wherein the electron trapping layer comprises silicon nitride.

17. The non-volatile memory cell as recited in claim 13, wherein the component stack further comprises a first dielectric layer and a second dielectric layer, and wherein the electron trapping layer is interposed between the first and second dielectric layers.

18. The non-volatile memory cell as recited in claim 13, wherein the component stack further comprises a second electrically conductive layer, and wherein the electron trapping layer is positioned between the second electrically conductive layer and the surface of the substrate.